



HC1243 FSK/OOK Transmitter Module

1. GENERAL:

The HC1243 is an ultra-low-cost, fully integrated FSK or OOK transmitter suitable for operation between 310 and 450 MHz, 860 and 870 MHz, as well as 902 and 928 MHz. For applications where economy is paramount, the HC1243 may be used without the requirement for configuration via an MCU. However, in conjunction with a microcontroller the communication link parameters may be re-configured. Including, output power, modulation format and operating channel.

The HC1243 offers integrated radio performance with cost efficiency and is suited for operation in North America FCC Part 15.231, FCC Part 15.247 FHSS and Digital Modulation Techniques, 15.249, and Europe EN 300 220.

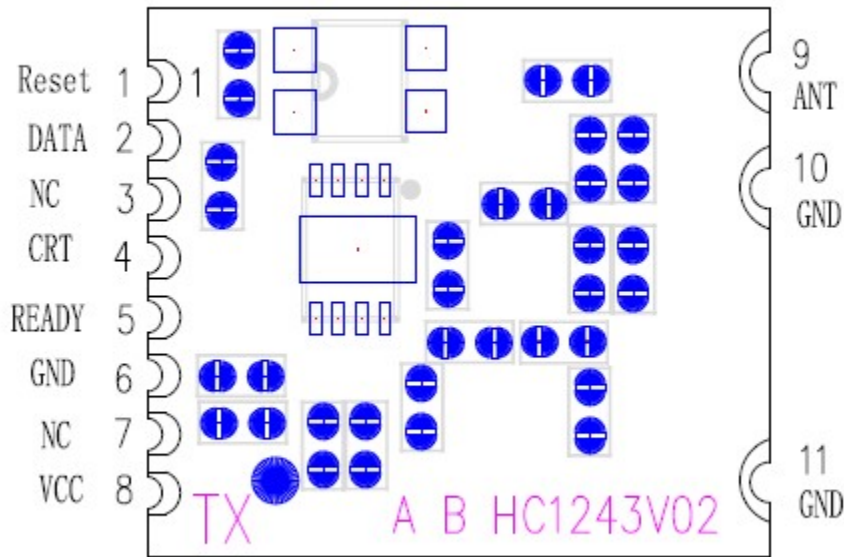
2. APPLICATIONS:

- ◆ Garage Door Openers
- ◆ Low-Cost Consumer Electronic Applications
- ◆ Remote Keyless Entry (RKE)
- ◆ Remote Control / Security Systems

3. FEATURES:

- ◆ +10 dBm or 0 dBm Configurable output power
- ◆ Bit rates up to 100 kbps
- ◆ OOK and FSK modulation.
- ◆ 1.8 to 3.7 V supply range.
- ◆ Low BOM Fully Integrated Tx
- ◆ Fractional-N PLL with 1.5 kHz typical step
- ◆ Frequency agility for FHSS modulation
- ◆ FCC CFR Part 15.247 Digital Modulation Techniques

4.PIN DESCRIPTION:



PIN No.	Name	I/O	Description
1	RESET	I	Module Hardware Reset, low pulse active
2	DATA	I/O	Transmit Data Transmit or Configuration Data
3	NC		Not connection
4	CRT	I	Config Selection Configuration Data Clock
5	READY	O	Transmitter Ready Flag (Optional, can be left floating)
6	GND	I	Module Power supply Negative, Groud
7	NC		Not connection
8	VCC	I	Module Power supply Positive
9	ANT	O	Module RF Output
10	GND	I	Module Power supply Negative, Groud
11	GND	I	Module Power supply Negative, Groud



5. Electrical Characteristics

5.1. ESD Notice

The HC1243 is an electrostatic discharge sensitive device. It satisfies Class 2 of the JEDEC standard



JESD22-A114-B (Human Body Model) on all pins.

5.2. Absolute Maximum Ratings

Stresses above the values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 2 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
VDDmr	Supply Voltage	-0.5	3.9	V
Tmr	Temperature	-55	115	° C
Tjunc	Junction Temperature	-55	125	° C
Tstor	Storage Temperature	-55	150	° C

5.3. Operating Range

Operating ranges define the limits for functional operation and the parametric characteristics of the device as described in this section. Functionality outside these limits is not implied.

Table 3 Operating Range

Symbol	Description	Min	Max	Unit
VDDop	Supply voltage	1.8	3.7	V
Top	Operational temperature range	-40	85	° C
Clop	Load capacitance on digital ports	-	25	pF



HC1243

FSK/OOK Transmitter Module

5.4. Electrical Specifications

The table below gives the electrical specifications of the transmitter under the following conditions: Supply voltage VBAT = 3.3 V, temperature = 25 °C, $f_{XOSC} = 26$ MHz, $f_{RF} = 915$ MHz, 2-FSK modulation with $F_{dev} = \pm 10$ kHz, bit rate = 10 kbit/s and output power = +10 dBm terminated in a matched 50 Ohm impedance, unless otherwise specified.

Table 4 Transmitter Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
Current Consumption						
IDDSL	Supply current in Sleep mode		-	125		nA
IDDT_315	Supply current in Transmit mode at 315 MHz*	RFOP=+10dBm 50% OOK	-	11	-	mA
		RFOP=+10dBm FSK	-	15	-	mA
		RFOP=0dBm	-	9	-	mA
IDDT_915	Supply current in Transmit mode at 915 MHz*	RFOP=+10dBm FSK	-	17.5	-	mA
		RFOP=0dBm FSK	-	10.5	-	mA
RF and Baseband Specifications						
FBAND	Accessible Frequency Bands See details in Table 7.	Band 0, with FXOSC=22 MHz	310	-	450	MHz
		Band 0, with FXOSC=24 MHz	312	-	450	MHz
		Band 0, with FXOSC=26 MHz	338	-	450	MHz
		Band 1, with FXOSC=26 MHz	860 902	- -	870 928	MHz MHz
FDA	Frequency deviation, FSK		10	-	200	kHz
BRF	Bit rate, FSK	Permissible Range	0.5	-	100	kbps
BRO	Bit rate, OOK	Permissible Range	0.5	-	10	kbps
OOK_B	OOK Modulation Depth		-	45	-	dB
RFOP	RF output power in 50 Ohms in either frequency band	High Power Setting	7	10	-	dBm
		Low Power Setting*	-3	0	-	dBm
RFOPFL	RF output power flatness	From 315 to 390 MHz, 50 Ohms load	-	2	-	dB
DRFOPV	Variation in RF output power with supply voltage	2.5 V to 3.3 V	-	-	3	dB
		1.8 V to 3.7 V	-	-	7	dB
PHN	Transmitter phase noise	At offset:				
		100 kHz	-	-84	-	dBc/Hz
		350 kHz	-	-94	-	dBc/Hz
		550 kHz	-	-96	-	dBc/Hz
		1.15 MHz	-	-105	-	dBc/Hz
STEP_22	RF frequency step	FXOSC = 22 MHz, Band 0	-	1.34277	-	kHz
STEP_24	RF frequency step	FXOSC = 24 MHz, Band 0	-	1.46484	-	kHz
STEP_26	RF frequency step	FXOSC = 26 MHz, Band 0	-	1.58691	-	kHz
		FXOSC = 26 MHz, Band 1	-	3.17383	-	kHz



HC1243

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Symbol	Description	Conditions	Min	Typ	Max	Unit
FXOSC	Crystal Oscillator Frequency		-	22	-	MHz
			-	24	-	MHz
			-	26	-	MHz
DFXOSC	Frequency Variation of the XOSC	No crystal contribution	-	-	+/-25	ppm
Timing Specifications						
TS_TR	Time from Sleep to Tx mode	XTAL dependant, with spec'd XTAL	-	650	2000	us
TS_HOP0	Channel hop time in Band 0	315 to 390 MHz	-	250	500	us
TS_HOP1	Channel hop time in Band 1	Maximum hop of 26 MHz***	-	200	400	us
TOFFT	Timer from Tx data activity to Sleep	Programmable	-	2	-	ms
			-	20	-	ms
RAMP	PA Ramp up and down time		-	20	-	us
T_START	Time before CTRL pin mode selection.	Time from power on to sampling of CTRL **	-	200 us + TS_OSC	-	ms

* With different matching networks

** The oscillator startup time, TS_OSC, depends on the electrical characteristics of the crystal

*** From the last CTRL falling edge of the Frequency change instruction to transmitter ready (PA ramp up



HC1243

FSK/OOK Transmitter Moudule

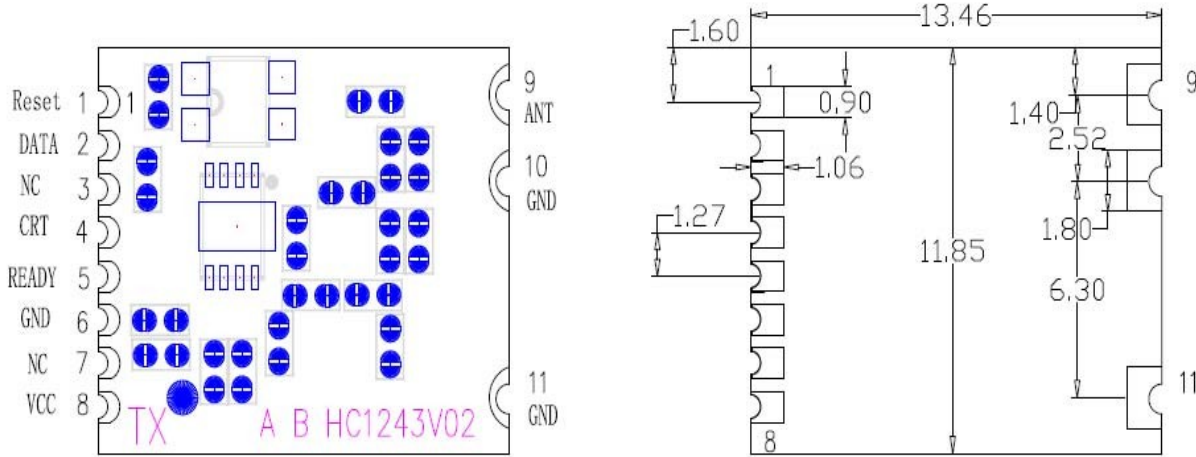
5.5. Digital Specification

The following table gives the operating specifications for the digital inputs and outputs of the SX1243.

Table 5 Digital Signals Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	Digital input level high		0.8	-	-	VBAT
V_{IL}	Digital input level low		-	-	0.2	VBAT
V_{OH}	Digital output level high	$I_{max} = 1 \text{ mA}$	0.9	-	-	VBAT
V_{OL}	Digital output level low	$I_{max} = -1 \text{ mA}$	-	-	0.1	VBAT
f_{CTRL}	CTRL Clock Frequency		-	-	10	MHz
t_{ch}	CTRL Clock High time		45	-	-	ns
t_{cl}	CTRL Clock Low time		45	-	-	ns
t_{rise}	CTRL Clock rise time		-	-	5	ns
t_{fall}	CTRL Clock Fall time		-	-	5	ns
t_{setup}	DATA Setup time	From Data transition to CTRL rising edge	45	-	-	ns
t_{hold}	DATA hold time	From CTRL rising edge to DATA transition	45	-	-	ns
t_0, t_2	Time at "1" on DATA during Recovery command	See Figure 10 and Figure 11	-	-	5	us
t_1	Time at "0" on DATA during Recovery command	See Figure 11	5	-	-	us

6. Module Package Outline Drawing: Unit: mm



7. Ordering Information:

Model	Part Number	Operation Band
HC1243	HC1243-315	315MHz
HC1243	HC1243-433	433MHz
HC1243	HC1243-868	868MHz
HC1243	HC1243-915	915MHz



8. Module Revisions:

Revisions	Date	Updated History
Rev1.0	March 2014	The first final release
Rev1.1	June 2015	Update Module parameter for 868MHZ. 915MHZ

9. Importance Notice:

The HC1243 datasheet will be changed by LJ ELECTRONICS TECHNOLOGY LIMITED according to the module design.

10. Contact us:

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