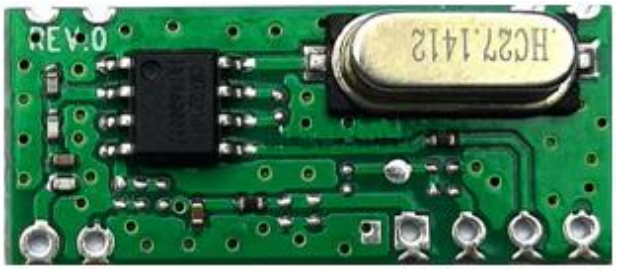
# Low Power 315MHz/433.92MHz OOK Receiver Module DATASHEET

## GENERAL DESCRIPTION

MDR2210H is a low power, high performance OOK RF receiver. It is suitable for ISM band 315MHz/433.92MHz wireless applications. The MDR2210H is a real plug and play chip without the register configuration or manual tuning. By selecting 19.7029MHz or 27.1412MHz crystal, the chip can operate at 315MHz or 433.92MHz. This chip supports the symbol rate range of 1~5 Kbps and is ideal for pairing with the low end transmitter based on the encoder or MCU. By selecting the VDD5V pin and VDDL pin open circuit or short circuit on the PCB, the MDR2210H can operate at two voltage ranges of 3.0V-5.5V or 2.0V-3.6V. When the chip operates at 433.92MHz, the receiver sensitivity of the -109dBm can be achieved with only 4.5mA current. The device is packaged in SOP8 to facilitate the simple and low cost manufacturing. MDR2210H receiver matching MDT110 transmitter can achieve the cost-effective RF application.

## KEY PRODUCT FEATURES

- Working frequency：315MHz/ 433.92MHz
- OOK demodulation
- Symbol rate：1.0 - 5.0 kbps
- Sensitivity：-109 dBm（3.0 kbps），0.1％BER
- Receiver bandwidth：330kHz
- Image rejection ratio：30dB
- Maximum input signal：10 dBm
- Run independently. Input from the antenna. Output the data.
- Configure without the register.
- Supply voltage (optional):
  - 3.0 – 5.5 V (High voltage mode)
  - 2.0 – 3.6 V (Low voltage mode)
- Low power consumption: 4.5 mA
- RoHS Compliant




## TYPICAL APPLICATIONS

- Low cost applications in the consumer electronics and appliances
- Automatic control of homes and buildings
- Infrared receiver replacement
- Industrial monitoring and control
- Wireless metering reading
- Wireless lighting control system
- Wireless alarm and security system
- Remote Keyless Entry (RKE)

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# 1 Electrical Characteristics

When $V_{DD}$= 3.3V， $T_{OP}$= 25 °C， $F_{RF}$ = 433.92 MHz， the sensitivity is measured by receiving a PN9 sequence and matching to 50Ω according to the 0.1%BER standard. All results are tested on the MDR2210H-EM unless otherwise stated.

## 1.1 Recommended Operating Conditions

Table1. Recommended Operating Conditions

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Operating supply voltage | VDD | When the VDD5V and VDDL are open-circuit, the temperature range is between -40 ℃and +85 ℃. | 3.0 | | 5.5 | V |
| | | When the VDD5V and VDDL are short-circuit, the temperature range is between -40 ℃and +85 ℃. | 2.0 | | 3.6 | V |
| Operating temperature | TOP | | -40 | | 85 | ℃ |
| Supply voltage slope | | | 1 | | | mV/us |

## 1.2 Absolute Maximum Rating

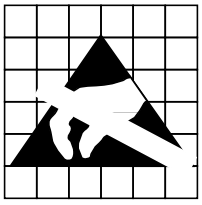
Table2.Absolute Maximum Rating[1]

| Parameter | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | VDD5V and VDDL are open-circuit. | -0.3 | 5.5 | V |
| | | VDD5V and VDDL are short-circuit. | -0.3 | 3.6 | V |
| Interface voltage | $V_{IN}$ | | -0.3 | $V_{DD}$ + 0.3 | V |
| Junction temperature | $T_J$ | | -40 | 125 | ℃ |
| Storage temperature | $T_{STG}$ | | -50 | 150 | ℃ |
| Welding temperature | $T_{SDR}$ | Last at least 30 seconds | | 255 | ℃ |
| ESD grade [2] | | Human Body Model (HBM) | -2 | 2 | kV |
| Latching current | | @ 85 ℃ | -100 | 100 | mA |

**Remarks：**

[1]. Exceeding the "absolute maximum rating" may cause the permanent damage to the device. This value is a pressure rating and does not mean that the equipment function is affected under this pressure condition. But if the device is exposed in the absolute maximum rating condition for a long time, its reliability may be affected.

[2]. MDR2210H is a high performance RF IC. The operation and assembly of this chip should only be performed on a workbench with good ESD protection.



**Warning! It is ESD sensitive device. In the operation of the chip, the user should pay attention to ESD precautions, so as to avoid the chip performance degradation or loss of function.**

## 1.3 Receiver

Table3. Receiver Specification

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Frequency range | $F_{RF}$ | $F_{XTAL}$ = 19.7029 MHz | | 315 | | MHz |
| | | $F_{XTAL}$ = 27.1412 MHz | | 433.92 | | MHz |
| Symbol rate | DR | | 1 | | 5 | kbps |
| Sensitivity | $S_{315}$ | $F_{RF}$ = 315 MHz, DR = 3 kbps, BER = 0.1% | | -109 | | dBm |
| | $S_{433.92}$ | $F_{RF}$ = 433.92 MHz, DR = 3 kbps, BER = 0.1% | | -109 | | dBm |
| Saturation input signal level | $P_{LVL}$ | | | 10 | | dBm |
| Working current | $I_{DD315}$ | $F_{RF}$ = 315 MHz | | 4.2 | | mA |
| | $I_{DD433.92}$ | $F_{RF}$ = 433.92 MHz | | 4.5 | | mA |
| Frequency synthesizer settle time | $T_{LOCK}$ | Start from XOSC stability | | 150 | | us |
| Anti blocking | BI | ±1 MHz, continuous wave interference | | 32 | | dB |
| | | ±2 MHz, continuous wave interference | | 42 | | dB |
| | | ±10 MHz, continuous wave interference | | 61 | | dB |
| Input 3rd order intercept point | IIP3 | FDEV = 1 MHz and 2 MHz double tone test, maximum system gain setting | | -23 | | dBm |
| Receiver bandwidth | $BW_{315}$ | $F_{RF}$ = 315 MHz | | 240 | | kHz |
| | $BW_{433.92}$ | $F_{RF}$ = 433.92 MHz | | 330 | | kHz |
| Receiver startup time [1] | $T_{START-UP}$ | From power up to receiving | | 4.5+$T_{XTAL}$ | | ms |

**Remarks:**

[1]. $T_{XTAL}$ is the oscillation time of crystal, which is related to the crystal itself and has nothing to do with the chip.

## 1.4 Crystal Oscillator

Table4. Crystal Oscillator Specification

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Crystal frequency [1] | $F_{XTAL315}$ | $F_{RF}$ = 315 MHz | | 19.7029 | | MHz |
| | $F_{XTAL433.92}$ | $F_{RF}$ = 433.92 MHz | | 27.1412 | | MHz |
| Crystal frequency accuracy [2] | | | | ±20 | | ppm |
| Load capacitance | $C_{LOAD}$ | | | 15 | | pF |
| Crystal equivalent resistance | Rm | | | | 60 | Ω |

| | | | | | | |
|---|---|---|---|---|---|---|
| Crystal start-up time [3] | $t_{XTAL}$ | | | 400 | | us |

**Remarks:**

[1]. MDR2210H can use the external reference clock to drive the XIN pin through the coupling capacitor. The peak value of the external clock signal is between 0.3 and 0.7 V.

[2]. The value includes (1) an initial error; (2) a crystal load; (3) aging; and (4) a change with the temperature. The acceptable crystal frequency error is limited by the receiver's bandwidth and the RF frequency deviation between the transmitter and the receiver.

[3]. The parameter is largely related to the crystal.

## 2 Pin Description

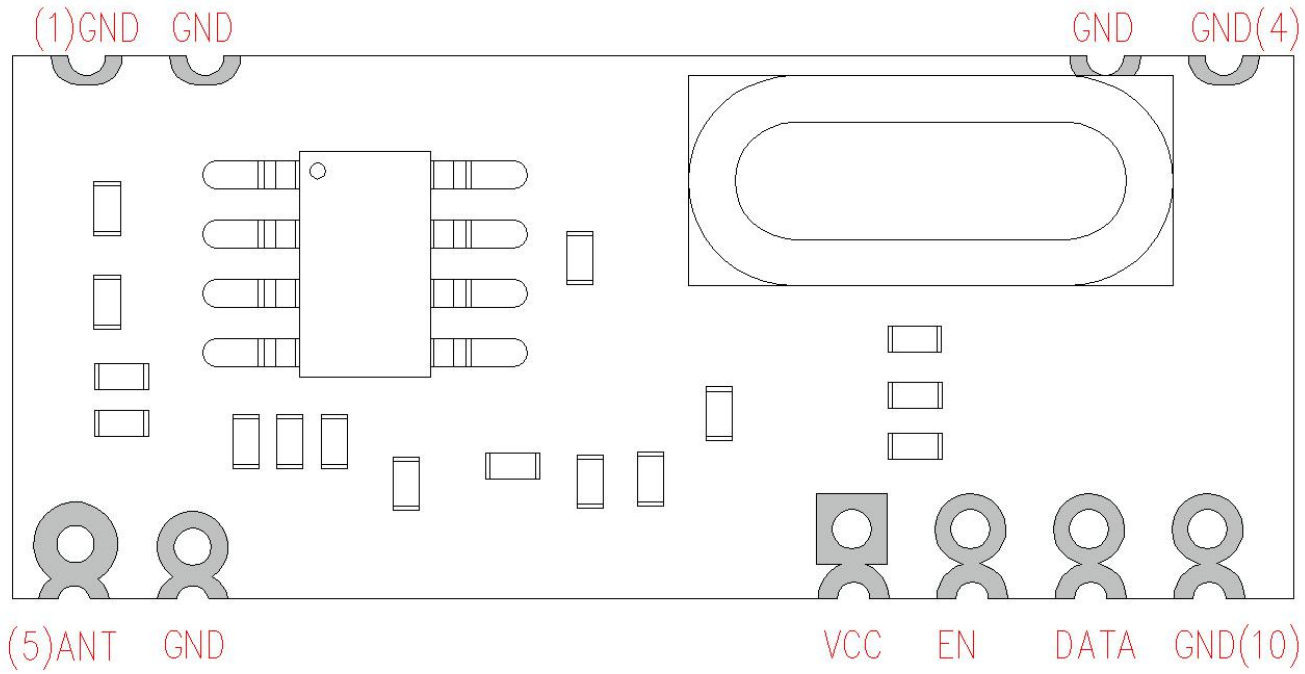



*Figure1. MDR2210H Pin Arrangement*

Table5. MDR2210H Pin Description

| Pin No. | Name | I/O | Function Description |
|---|---|---|---|
| 1,2,3,4,6,10 | GND | I | Power ground |
| 5 | ANT | O | Module Antenna terminal, Default terminal |
| 7 | VCC | I | Module power supply |
| 8 | EN | | DO not use |
| 9 | DATA | O | Received signal output |

## 3 Typical Performance

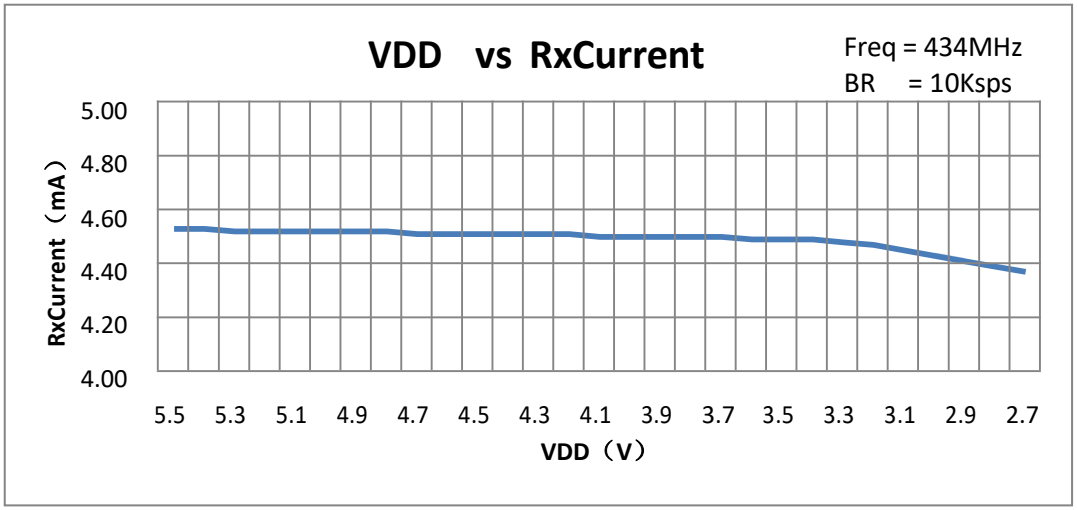



*Figure2. Rx Current vs Supply Voltage*

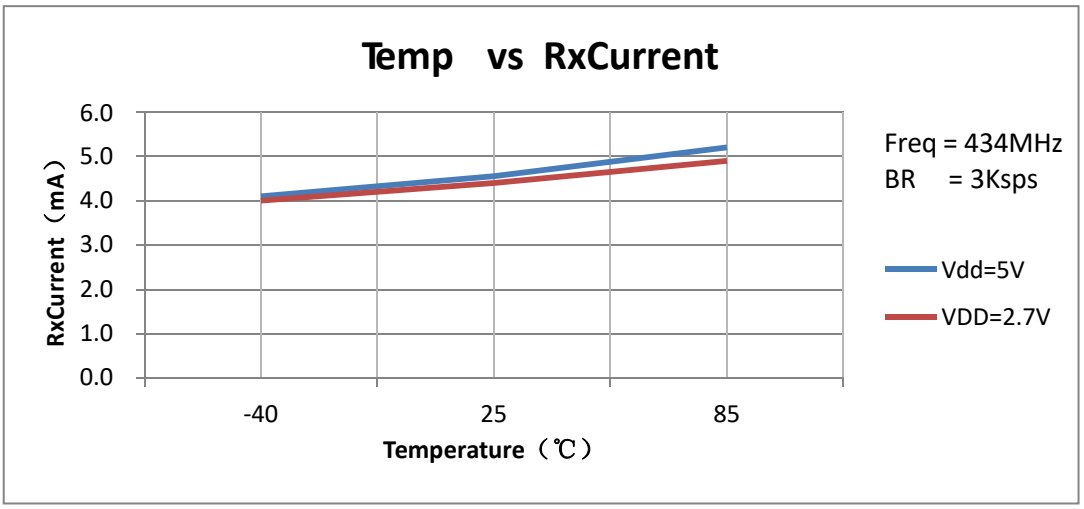



*Figure3. Rx Current vs Working Temperature*

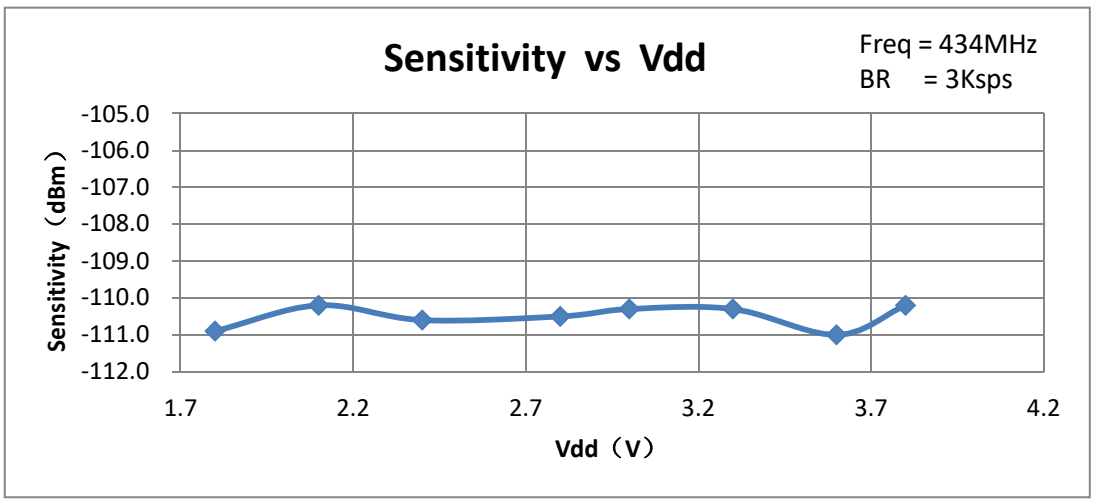



*Figure4. Sensitivity vs Supply Voltage*

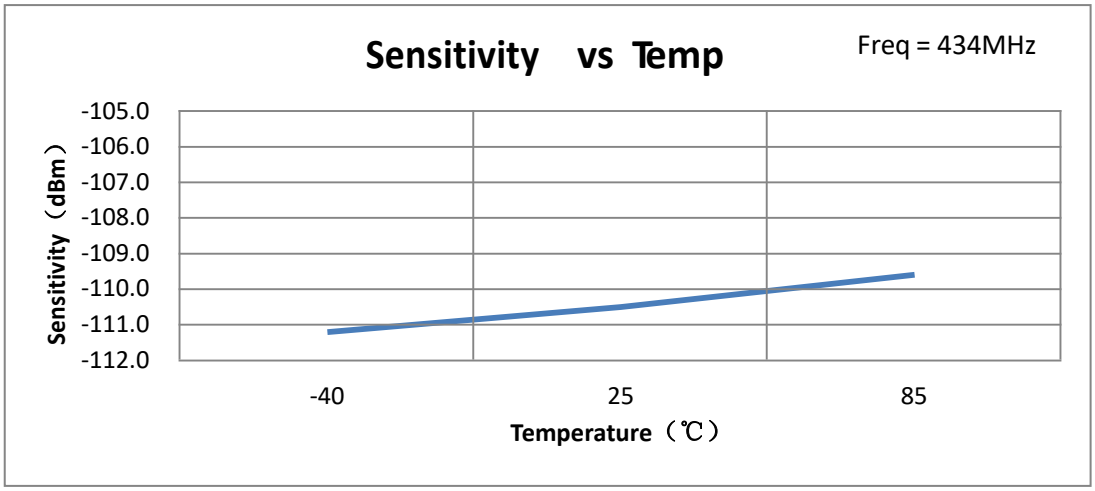



*Figure5. Sensitivity vs Working Temperature*

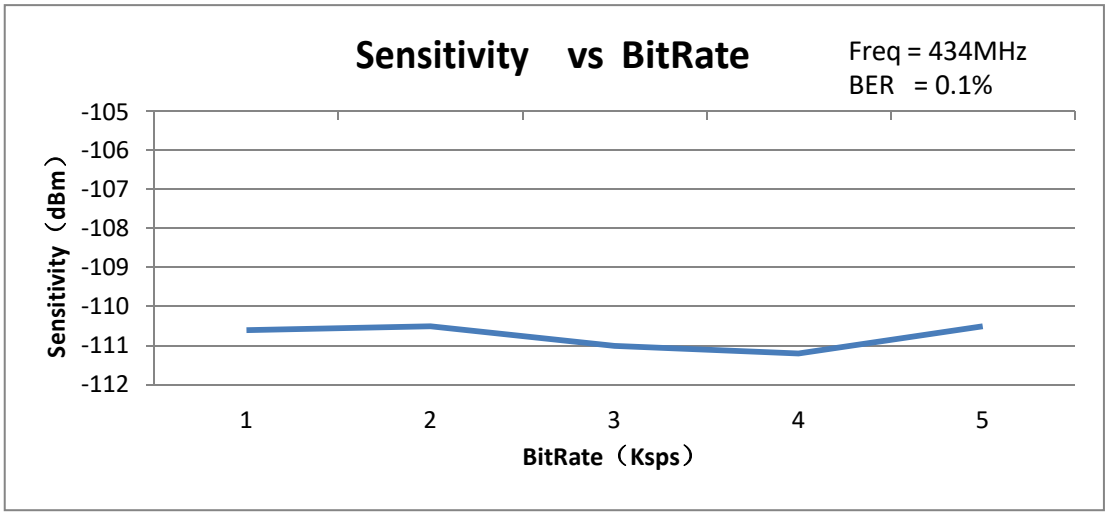



*Figure6. Sensitivity vs Bit Rate*

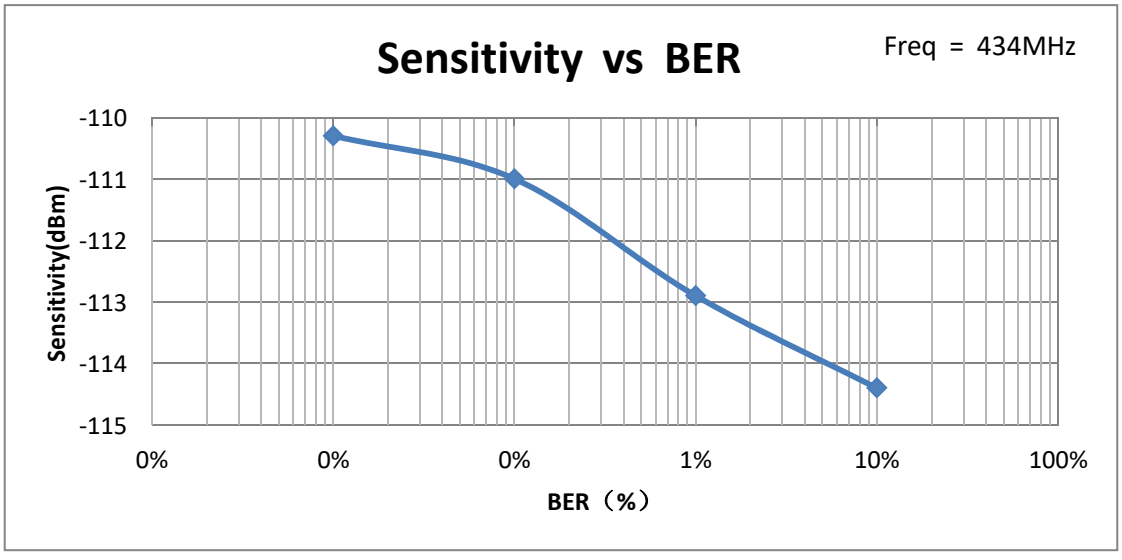



*Figure7. Sensitivity vs Bit Error Rate*

## 4 Typical Application Schematic Diagram

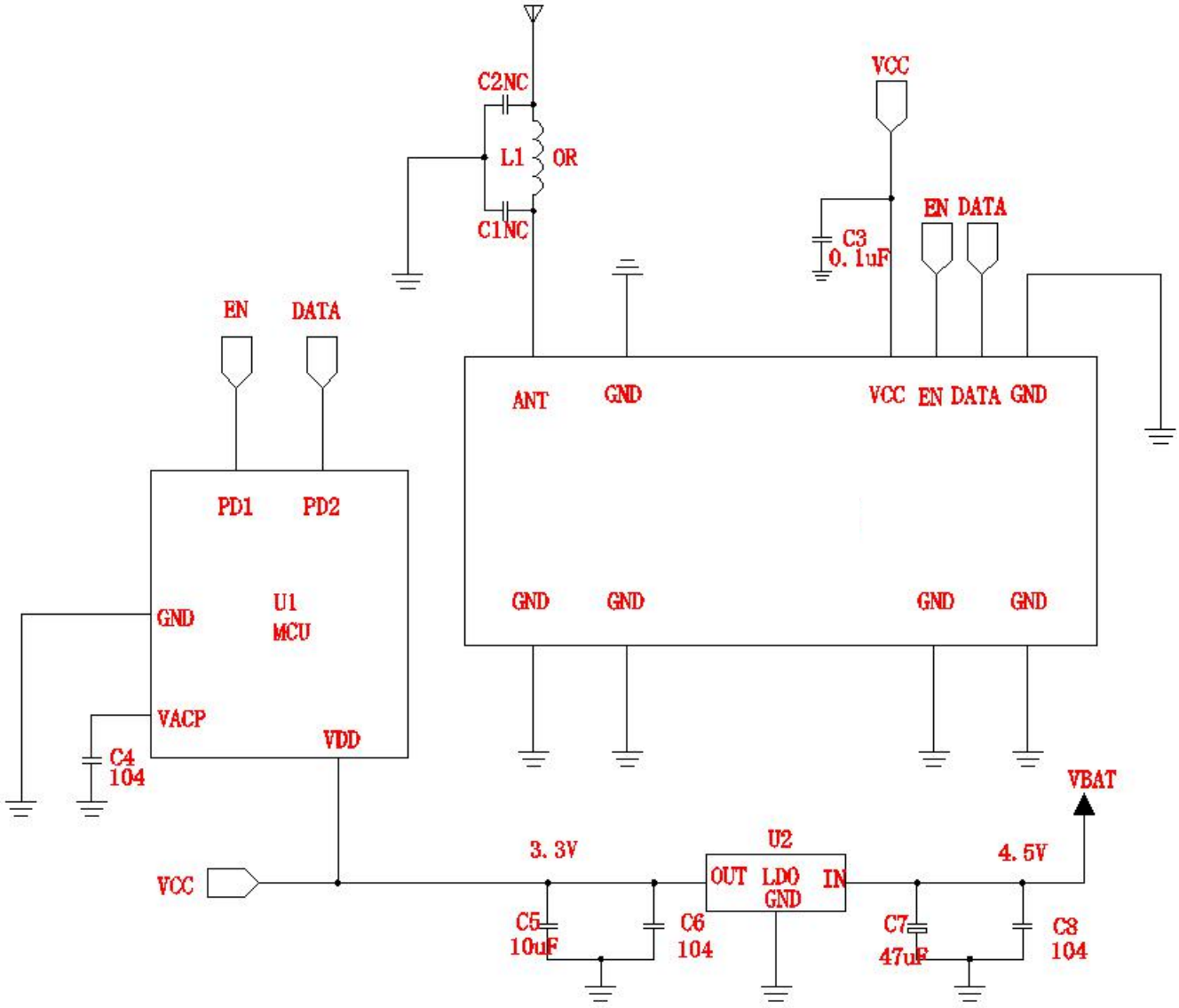



*Figure8. Typical Application Schematic Diagram*

Table6. BOM matching the 315MHz / 433.92MHz typical application

| Designator | Descriptions | Manufacturer |
|---|---|---|
| M1 | Module MDR2210H 27.44*11.65*5mm RoHS | PANZHI TECH ELECTRONICS |
| U1 | IC 8 BIT MCU STM8S003F3 SSOP20 RoHS | MICROICHIP |
| U2 | IC LDO XC6206P33PR 3.3V SOT-23 RoHS | TOREX |
| L1 | Thick film resistor0R 5% 1/16W 0402 RoHS | ROHM |
| C1 | CAP CER 0402 DO NOT FIT | |
| C2 | CAP CER 0402 DO NOT FIT | |
| C3 | CAP CER 0.1uF/25V 20% X7R 0402 RoHS | MURATA |
| C4 | CAP CER 0.1uF/25V 20% X7R 0402 RoHS | MURATA |
| C5 | CAP CER 10uF/16V 20% X5R 0402 RoHS | MURATA |
| C6 | CAP CER 0.1uF/25V 20% X7R 0402 RoHS | MURATA |
| C7 | CAP CER 47uF/16V 20% X5R 1206 RoHS | MURATA |
| C8 | CAP CER 0.1uF/25V 20% X7R 0402 RoHS | MURATA |

# 5 Function Descriptions:

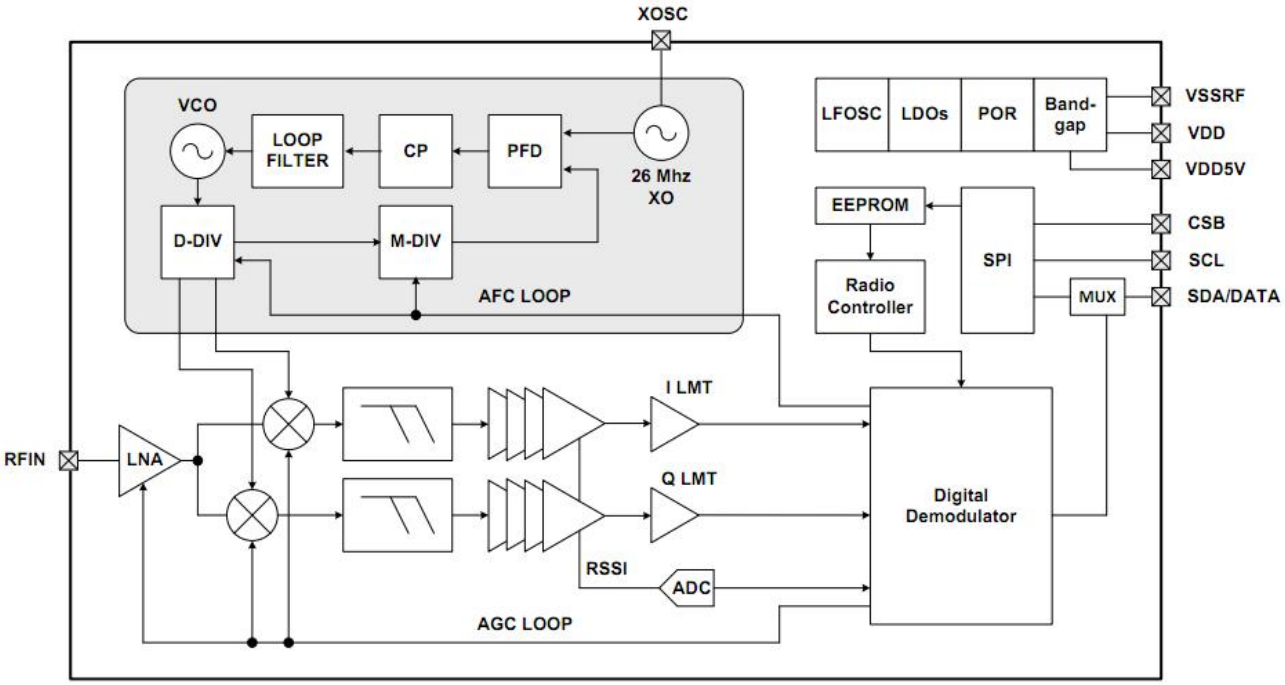



*Figure9. Function Module Diagram*

## 5.1 Summary

MDR2210H is a digital-analog hybrid receiver. The product adopts the 26MHz crystal to provide the reference frequency and digital clock for PLL, supports OOK demodulation output with the data rate of 1.0-5.0Ksps, and supports the periodic reset with the configurable time to avoid the crash phenomenon caused by various external reasons. MDR2210H supports two kinds of voltage, which can be used in the application of 5V system, and also can be chosen as the application of 3V system.

The chip uses LNA+MIXER+IFFILTER+LIMITTER+PLL's low intermediate frequency structure to achieve the wireless reception function below Sub-1G frequency. The analog front-end is responsible for mixing RF signals into intermediate frequency, and converting the real time RSSI into the 8-bit digital signal through SAR-ADC, and sending them to the interior to do the OOK demodulation and correlation processing. At the same time, the internal circuit will mix the intermediate frequency signal down to the zero frequency

(Baseband) and do a series of filtering and judging process, while AGC dynamically control the analog front-end. Finally, the original signal is demodulated and output through the DATA pin.

The parameters of the chip are stored in an internal EEPROM, and the user can modify or adjust the working parameters of the chip by the RFPDK.

## 5.2 Demodulation Mode, Frequency and Symbol Rate

MDR2210H supports the OOK demodulation of 1.0-5.0ksps symbol rate. It supports for free ISM bands near 315 MHz and 433.92MHz. The following table gives the information about the demodulation mode, frequency and symbol rate of the MDR2210H.

Table 7. Demodulation mode, frequency and symbol rate

| Parameter | Value | Unit |
|---|---|---|
| Demodulation mode | OOK | - |
| Frequency | 315 / 433.92 | MHz |
| Symbol rate | 1.0–5.0 | Ksps |

## 5.3 Function Module Description

### 5.3.1 RF Front-end and Automatic Gain Control

MDR2210H is an OOK modulated receiver with the low intermediate frequency architecture. The receiver's RF front-end consists of a low noise amplifier (LNA), an I / Q mixer (Mixer), an intermediate frequency filter (IF Filter), and a wideband power detector (WB Power Detector). The RF front-end amplifies and converts the RF input signals from the antenna to the intermediate frequency for the further processing.

With the help of the broadband power detector and RF attenuation network of RF front-end, the automatic gain control (AGC) loop can adjust the RF front-end gain. The chip can also achieve the best system linearity, selectivity and sensitivity even under the condition of strong interference outside the band.

With only one low-cost matching circuit, the LNA input can be matched to 50Ω or other types of antennas.

### 5.3.2 Intermediate Frequency (IF) Filter

The signal from the RF front-end is filtered by an integrated 3rd order band pass image rejection filter. When the device operates at 433.92 MHz, the intermediate frequency bandwidth is 330 kHz. The center frequency and bandwidth will be adjusted automatically according to the selected crystal frequency.

### 5.3.3 Received Signal Strength Indicator

The output signal of the IF filter is amplified by the cascade I/Q logarithmic amplifier, and then sent to the

demodulator for demodulation. I/Q dual logarithmic amplifiers include the received signal strength indicator (RSSI). The indicator generates the DC level in proportion to the input signal level within the I/Q path. The sum of levels of these two paths is used as an indication of the received signal strength, with a dynamic range of more than 66dB.

### 5.3.4 Successive Approximation Register

The 8-bit SAR-ADC in MDR2210H transforms the RSSI output into the digital signal for OOK demodulation.

### 5.3.5 Crystal Oscillator

MDR2210H uses a single ended crystal oscillator circuit with the required load capacitance integrated within the chip. The recommended crystal is 19.7029MHz/27.1412MHz, with an accuracy of + 20 ppm, an equivalent resistance (ESR) <60 and a load capacitance (CLOAD) of 15pF. In order to save the external load capacitance, the load capacitance required by the crystal oscillation is integrated in the MDR2210H chip.

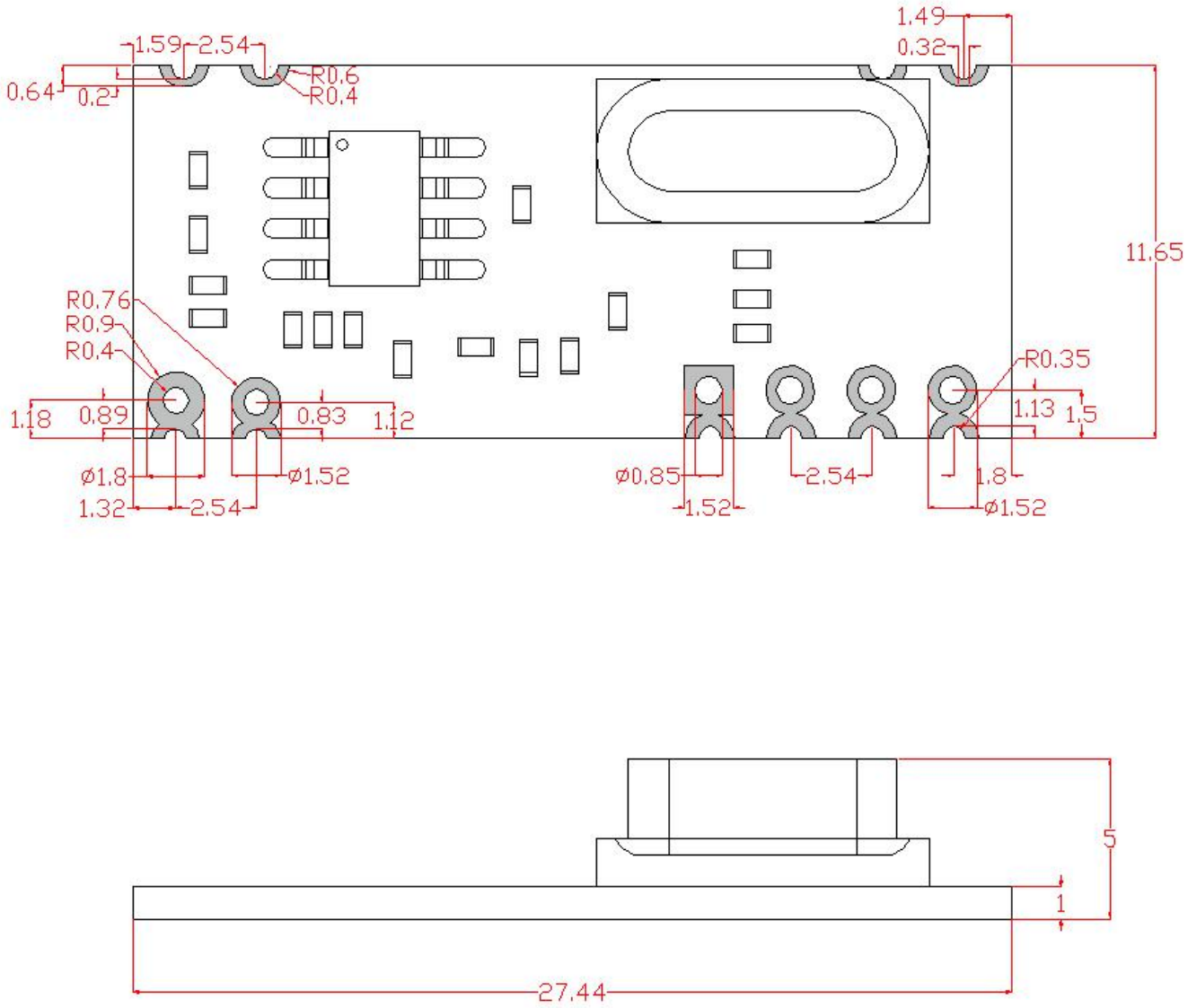
If there is a suitable clock source (RCLK) in the application system, which can be used as the reference clock of MDR2210H, the user can drive the XIN pin of the chip through the DC blocking capacitor. This will save one crystal and further reduce the system cost. The recommended RCLK peak to peak value is between 0.3V to 0.7V (at the XTAL pin).

### 5.3.6 Frequency Synthesizer

The frequency synthesizer is used to generate the local oscillator (LO) frequency required for the I/Q mixer. By the 19.7029 MHz or 27.1412 MHz reference clock provided by a crystal or external clock source, the frequency synthesizer can generate the 315MHz /433.92MHz working frequency. The internal high performance VCO operates at the 2x LO frequency without the external inductor. The chip can work stably in various conditions when it is powered up, and further save the system power consumption and stray radiation.

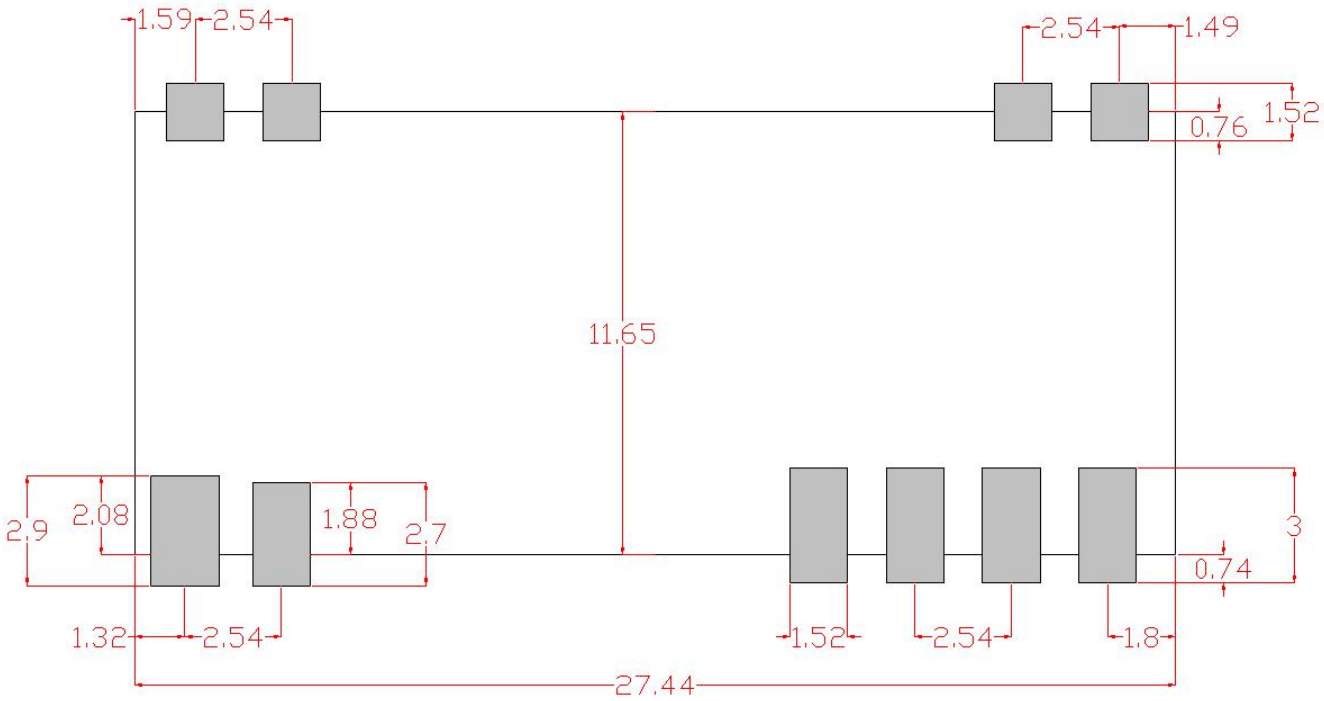
## 6 Module Package OutlineDrawing

Unit: mm



## 7 Recommended PCB Land Pattern

Unit: mm




## 8 Tray Packaging

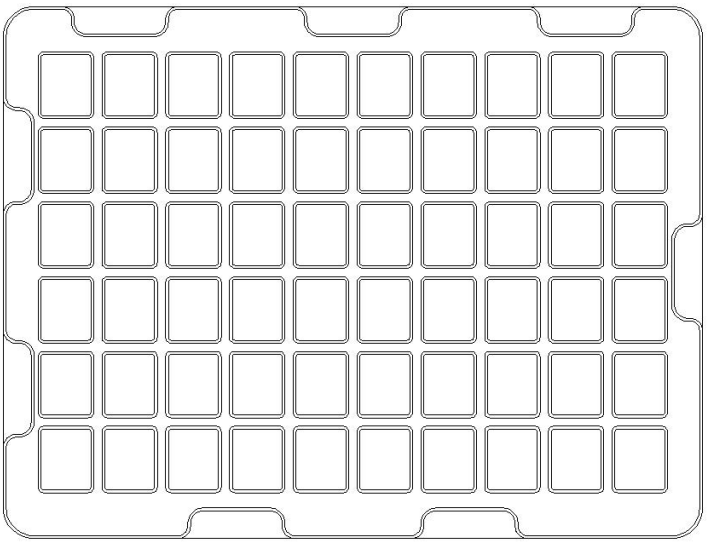
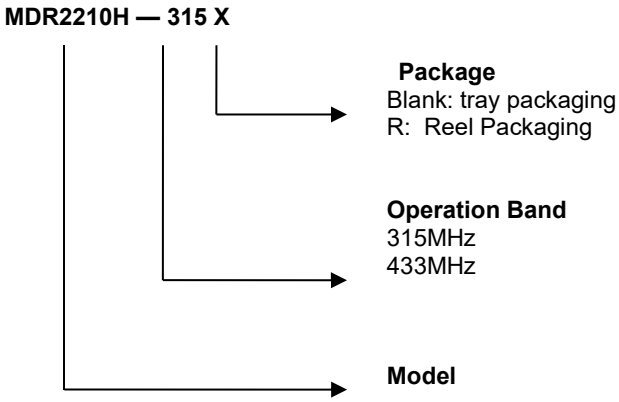


*Figure10. Package Outline Drawing*

*Note:*

*tray packaging, 60pcs/tray.*

# 9 Ordering Information:




# 10 Module Revisions:

Table8 Revision History

| Revisions | Date | Updated History |
|---|---|---|
| Rev 1.0 | April 2017 | The first release |

## 11 Contact us:

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