Sub GHz ASK/OOK Receiver Module DATASHEET

GENERAL DESCRIPTION

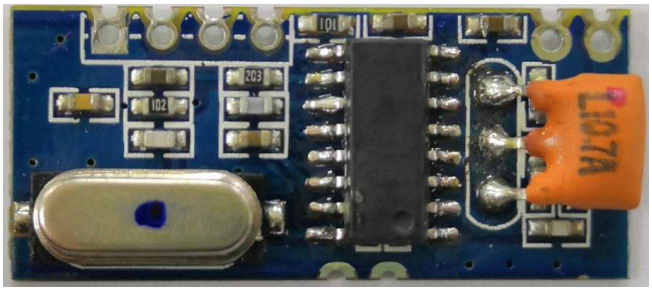
MD303M is one low power direct-conversion OOK/ASK receiver. The circuit is mainly intended for the ISM (Industrial, Scientific and Medical) band 315/433MHz, It is designed for low cost data transmission system for data rate less than 20Kb/s in Manchester.

MD303M integrates most circuit components on-chip and only requires a few external components to work normally. The MD303M consists of a low-noise amplifier (LNA), a down-conversion mixer, an on-chip phase-locked loop (PLL) with integrated voltage-controlled oscillator (VCO) and loop filter, an ASK demodulator, a data filter, a data slicing comparator and an on-chip regulator.

The MD303M is designed for low power and low voltage wireless applications. It is available in SOP-16 package and working over the extended temperature range (-40 to +85°C).

KEY PRODUCT FEATURES

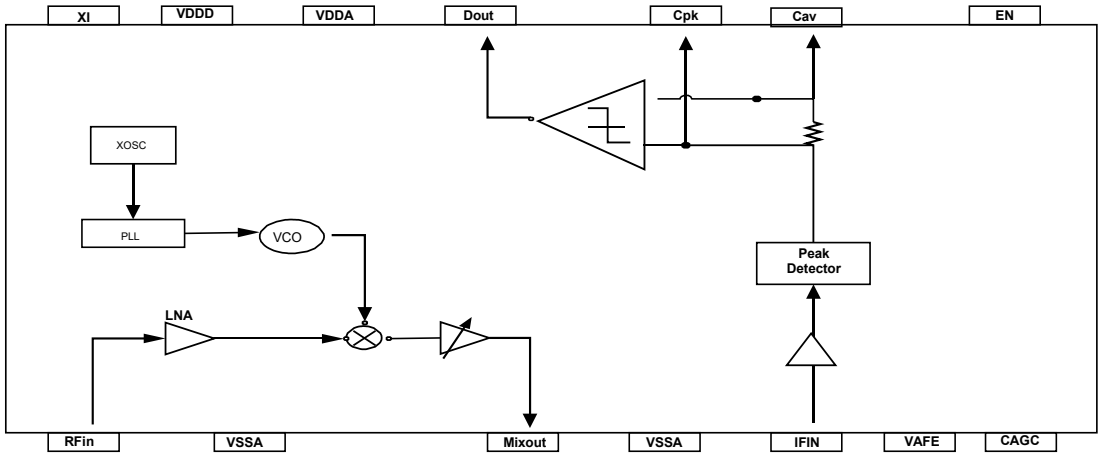
- Low power consumption: 3.5mA for 315/433 MHz
- Low supply voltage: 2.2V-5.5V for 315/433MHz
- Excellent Sensitivity of the order of -110dBm (peak ASK signal level)
- 200 MHz to 500 MHz frequency range
- Data rate up to 40Kb/s



APPLICATIONS

- Remote Keyless Entry (RKE)
- Remote Control, Garage door and gate openers
- AMR-Automatic Meter Reading
- Wireless alarm and security system
- 315/433MHz ISM band system

Block Diagram



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1 Pin Diagram

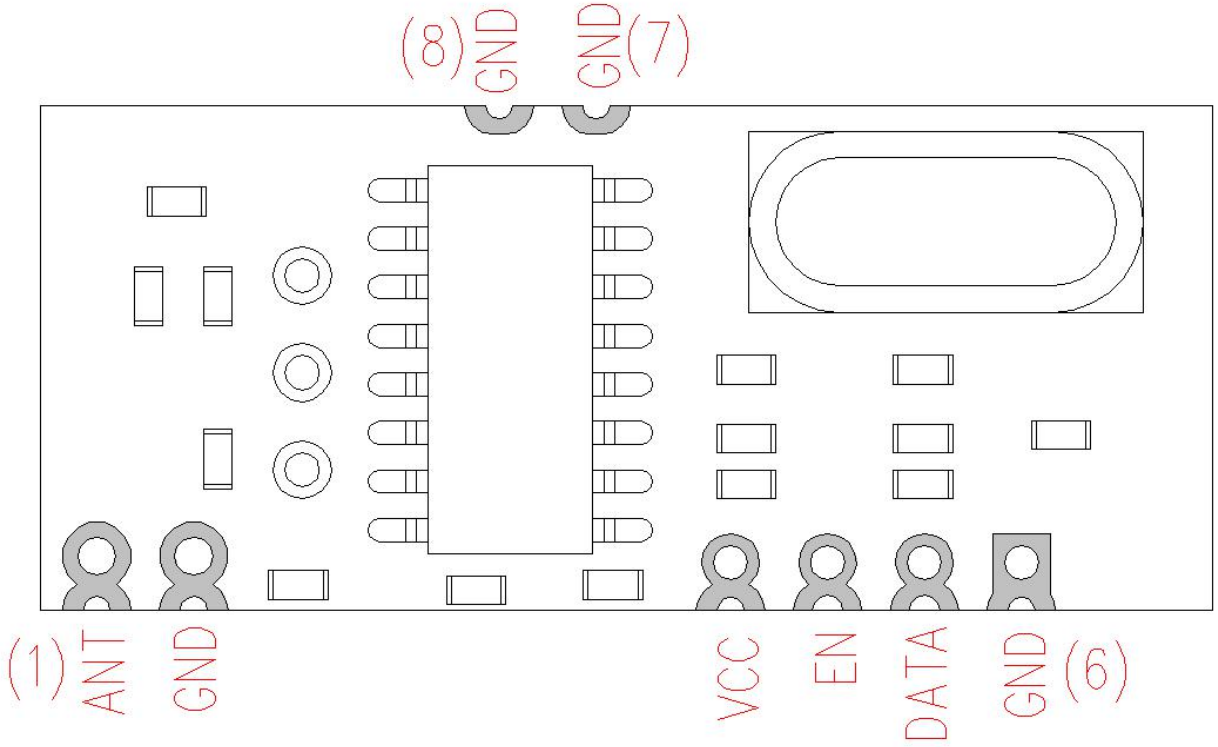


Table 1. Pin Description

Pin Number	Pin Definitions	Description
1	ANT	Connect with 50 ohm coaxial antenna
2	GND	Connected to power ground
3	VCC	Positive power supply
4	EN	1: Normal working 0: Sleep mode
5	DATA	Data output
6,7,8	GND	Connected to power ground

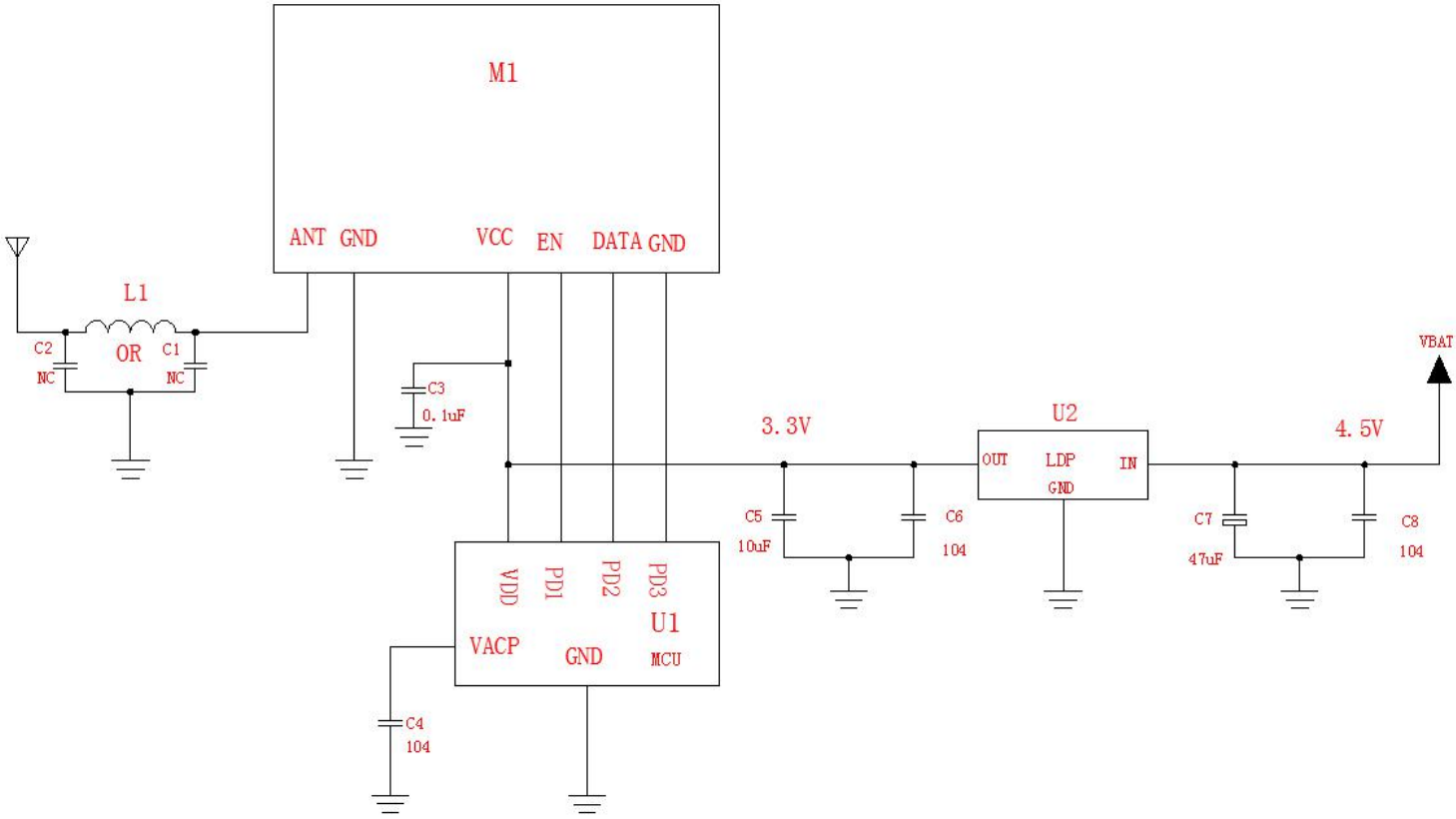
Table 2. Absolute Maximum Rating

Item	Rating
Supply Voltage, VDD	+ 6.0V
Inputs and Clock Outputs	- 0.5V to + 6.0V
Storage Temperature	- 65 °C to + 150 °C
Soldering Temperature	+ 260 °C

Table 3. Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Regulated Voltage	V_{DDA}			2.6		V
Supply Voltage	V_{DDD}	200MHz-500MHz	2.2	3.0	5.5	V
Supply Current	I_{DD}	Fin=315MHz , 3V		3.5		mA
		Fin=434MHz , 3V		3.6		mA
FIN operating Frequency	Fin		200		500	MHz
FIN Sensitivity	V_{FIN}	Fin=315MHz		-110		dBm
		Fin=433MHz		-110		dBm
OSCI operating Frequency	F_{OSC}		9		25	MHz
OSCI Input Voltage	V_{OSCI}		-10	0	5	dBm
Operating Temperature	T_a		-40		85	℃
Leakage Current	I_{SB}	Power down mode			1	uA

2 Application Information



Designator	Descriptions	Manufacturer
M1	Module MD303M 30.72*13.21*5mm RoHS	PANZHI TECH ELECTRONICS
U1	IC 8 BIT MCU STM8S003F3 SSOP20 RoHS	MICROICHIP
U2	IC LDO XC6206P33PR 3.3V SOT-23 RoHS	TOREX
L1	Thick film resistor0R 5% 1/16W 0402 RoHS	ROHM
C1	CAP CER 0402 DO NOT FIT	
C2	CAP CER 0402 DO NOT FIT	
C3	CAP CER 0.1uF/25V 20% X7R 0402 RoHS	MURATA
C4	CAP CER 0.1uF/25V 20% X7R 0402 RoHS	MURATA
C5	CAP CER 10uF/16V 20% X5R 0402 RoHS	MURATA
C6	CAP CER 0.1uF/25V 20% X7R 0402 RoHS	MURATA
C7	CAP CER 47uF/16V 20% X5R 1206 RoHS	MURATA
C8	CAP CER 0.1uF/25V 20% X7R 0402 RoHS	MURATA

3 Functional Description

3.1 Crystal Oscillator (Pin 16)

The crystal oscillator circuit consists of a colpit oscillator. Pin 16 can drive one off-chip 9MHz-25MHz

The crystal driver stage can also take input clock as input clock buffer. The crystal oscillator frequency is determined as follows

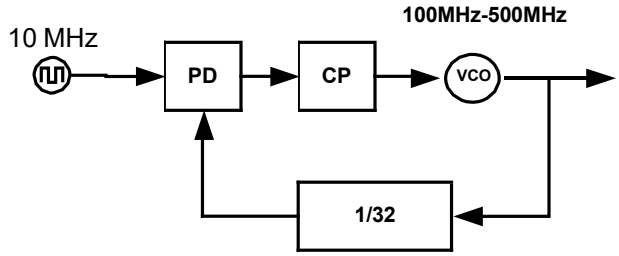
fosc= fvco / N = (ftx +/- 10.7) / N

Where Fvco is VCO oscillation frequency. Ftx is the transmitted/received signal frequency. 10.7MHz is super-heterodyne receiver IF frequency. N is the divider ration of PLL block.

3.2 PLL Block

The below figure shows the PLL block diagram. The PLL consists of phase-frequency detector (PFD), charge pump, loop filter, voltage-controlled oscillator (VCO), and divider (1/32). The PFD compares two signals and produces an error signal which is proportional to the two signal phase difference. The error signal is used to control the VCO to run fast or slow.

The VCO oscillation frequency range is tunable between100MHz-500MHz,

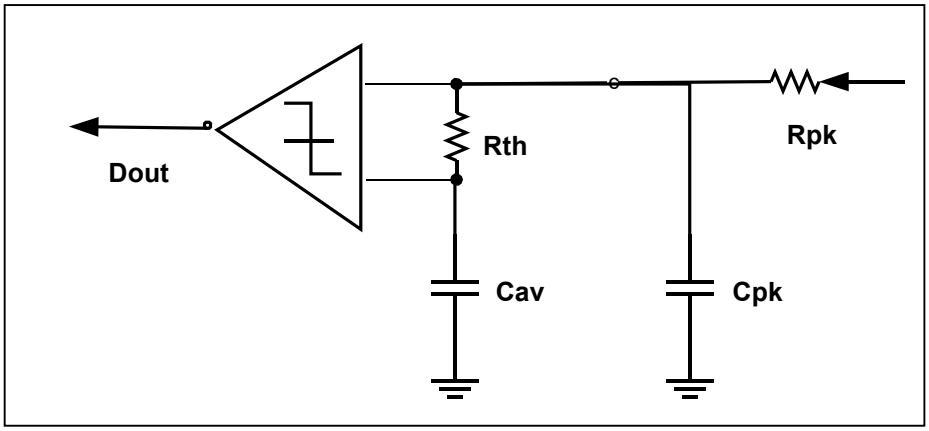


3.3 Peak-Detector & ASK Demodulator

The peak-detector detects the HIGH and LOW modulated ASK signal level. The ASK demodulation is done by data slicer.

The data slicer takes the input analog signal from peak detector and determines the input signal is HIGH or LOW. The reference level for data slicer slicing is the long-term average of peak-detected signal, using the external threshold capacitor **C_{AV}** (pin 10) and the on-chip resistor R_{TH}, which is about **30KΩ**. The Slicing level time constant values (**$\tau = C_{AV} * R_{TH}$**) can be set around 20X bit period time.

To reduce the variation of peak-detected signal, an external capacitor **C_{pk}** (pin 11) is used to reduce the ripple. The time constant values (**$\tau = C_{pk} * R_{pk}$**) can be set around 1X bit period time. The internal resistance **R_{pk}** is around **60K.**



For 2Kb/s data rate, the typical value **C_{AV}=4700nF, C_{pk}=2nF.**

Below table is suggested capacitor value for different data rate.

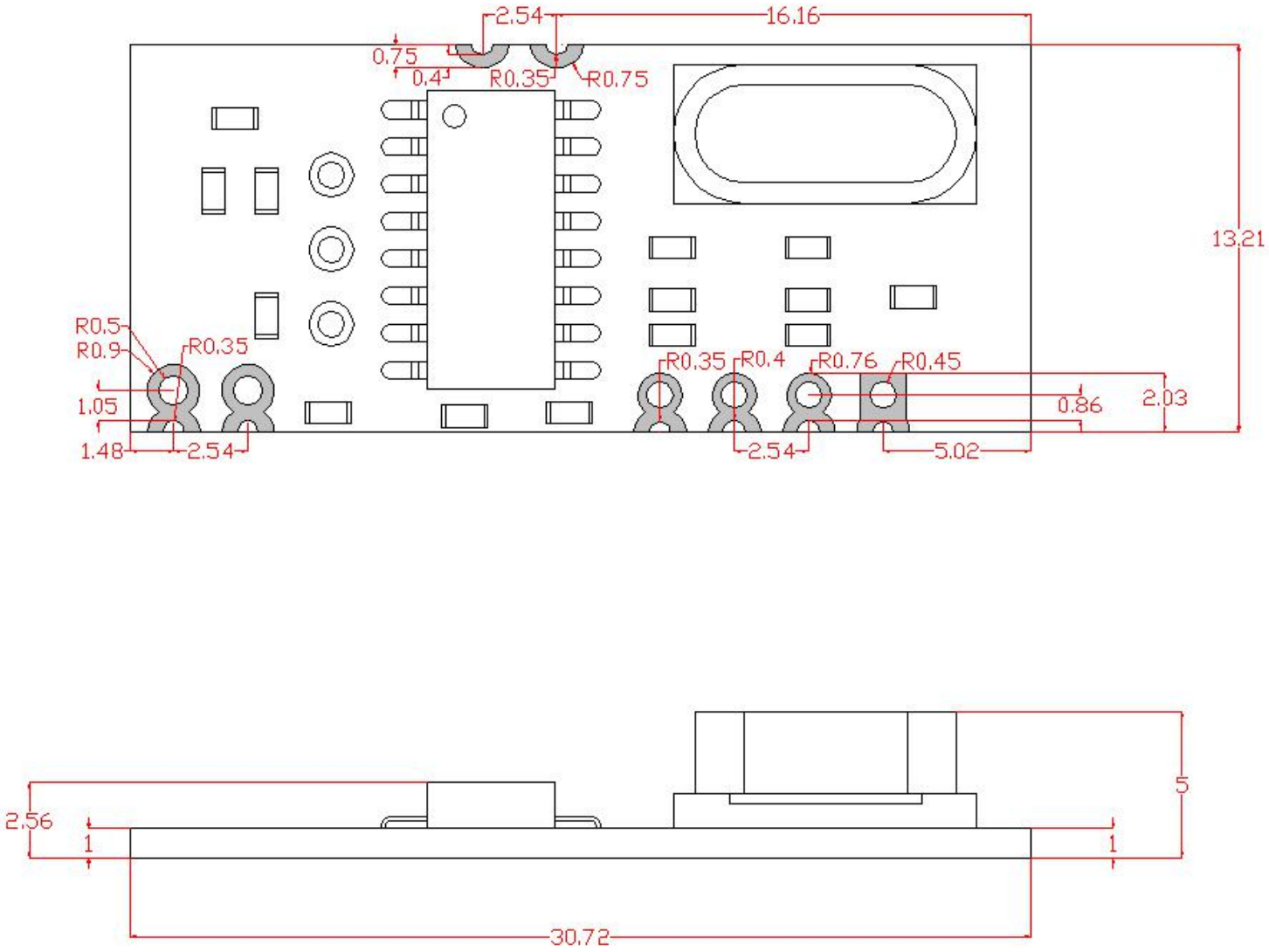
Slicer cap	Bit Rate		Note
	10Kb/s	2KB/s	
Cav	1000n	4700n	
Cpk	0.47n	2n	

3.4 AGC Loop

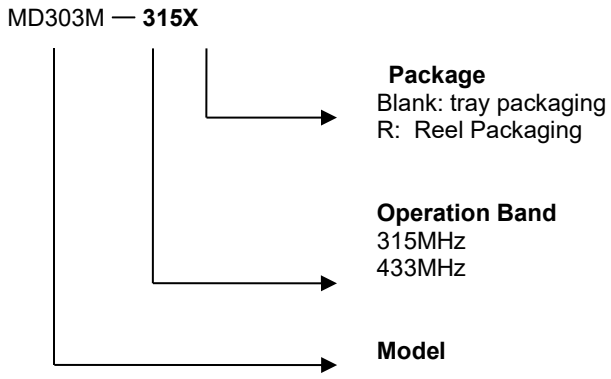
The AGC loop compares HIGH signal level with average signal. When the signal difference is larger than 50mV, the AGC loop reduces the analog front end (AFE) stage gain. The external capacitor Cagc controls the AGC loop response time.

4 Module Package OutlineDrawing

Unit: mm



5 Ordering Information:



6 Module Revisions:

Table 4 Revision History

Revisions	Date	Updated History
Rev1.0	April 2015	The first final release
Rev1.1	April 2016	Add product pictures

7 Contact us:

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